REMARKS/ARGUMENTS

Reexamination and reconsideration of this application as amended is requested. By this amendment, claims 1, 3-4, 6-7, 17-18, and 20 have been amended. Claims 1-20 remain in the application.

REJECTION OF CLAIMS 1-4 UNDER 35 U.S.C. §103

Claims 1-4 have been rejected under 35 U.S.C. 103 as being unpatentable over Yaung et al.

Yaung et al. shows a method of forming a CMOS image sensor device including a sensor diode 116/110 wherein source/drain regions are implanted into one terminal 116 of the sensor diode. The sensor diode occupies a portion of the integrated circuit area of the chip as viewed from "above", being integrated at the same level as the transistors and the like.

The Examiner has stated there is a sensor diode in the substrate and a photosensing element (a photodiode 116) fabricated in a vertically integrated active layer. These diodes are the same diode, being the junction between 116 and the substrate 110. It is formed in the same layer 114 as the transistors identified by the gates 166 and 170. This is not vertical integration as the term is used by those skilled in the art. And the diode 116/110 does not surround the vertical interconnect - it is positioned below the vertical interconnect. Furthermore, there is no lateral flow to the "side" of the interconnect.

The present invention teaches a vertically integrated photosensor wherein circuitry is integrated onto a substrate, and the photosensor is positioned over the circuitry and coupled thereto by a via. One of an n-type or p-type material is positioned between the via and the other of the one of an n-type or p-type material, with this p-n junction positioned between the via and

photosensitive material. This arrangement provides for the charge carriers to be "drawn toward the axis of said vertical interconnect". Furthermore, this placement of the photosensor and circuitry into different layers allows for independent optimization of photosensor device performance and system architectural design. For the photosensor, this may include, for example: choice of materials; pixel design (optical and electronic); fabrication processes resulting in detectors with much higher fill factors (on the order of about 3-4x greater); and/or the like. The utilization of the third dimension substantially obviates competition for lateral pixel area and also allows greater functionality to be incorporated into any given 2D form factor. The underlying electronics may then be designed effectively without compromise from the optical coupling requirements of the photosensor. This generally allows for the use of much needed additional layers of interconnect metallization for more efficient layout of chips and also opens the door for the incorporation of greater image processing functions on-chip with more creative architectural partitioning of the imaging system potentially leading to single-chip camera applications.

The cited Yaung et al. reference shows integrating the sensor diode within the circuitry, while the present invention teaches the vertical placement of the sensor on top of the circuitry. The present invention therefore has more area for the transistors and the like in the electronics layer and also much more area in the sensor for collection of photons.

It would not be obvious to one skilled in the art with knowledge of Yeung (a n-p junction formed on the same level as the transistors and the like) to construct the device of the present invention where a monocrystalline photosensing element is bonded to an electronics layer, and a junction within the monocrystalline photosensing element includes (in amended claim 1) one of a p-type and an n-type material having a first side adjacent said vertical

interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

More specifically, Claim 1 as amended comprises a monocrystalline photosensing element that is bonded to the electronics layer. Furthermore, the junction within the monocrystalline photosensing element now includes (in amended claim 1) one of a p-type and an n-type material having a first side adjacent said vertical interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

Claims 2-4 are believed to be allowable at least for the reason they depend from what is believed to be an allowable claim.

Claim 4 has been amended to reflect that the optically active layer is monocrystalline as added to claim 1.

Accordingly, it is believed that the rejection of claims 1-4 under 35 U.S.C. 103 has been overcome by the amendment and remarks.

REJECTION OF CLAIM 5 UNDER 35 U.S.C. §103

Claim 5 has been rejected under 35 U.S.C. 103 as being unpatentable over Yaung et al. in view of Tsai et al.

The Tsai cited reference shows a photosensitive semiconductor package wherein a photosensitive semiconductor chip 25 is mounted on the chip carrier 20.

The chip 25 is not electrically connected to the chip carrier 20, and there is no mention of placing (monolithically integrating) a sensor vertically on top of circuitry and connecting them together electrically.

As stated above, the present invention teaches a vertically integrated photosensor wherein circuitry is integrated onto a substrate, and the photosensor is positioned over the circuitry and coupled thereto by a via. One of an n-type or p-type material is positioned between the via and the other of the one of an n-type or p-type material, with this p-n junction positioned between the via and photosensitive material. This arrangement provides for the charge carriers to be "drawn toward the axis of said vertical interconnect". Furthermore, this placement of the photosensor and circuitry into different layers allows for independent optimization of photosensor device performance and system architectural design.

It would not be obvious to one skilled in the art with knowledge of Yeung (a n-p junction formed on the same level as the transistors and the like) and Tsai (a sensor bonded to a chip carrier without any circuitry) to construct the device of the present invention where a monocrystalline photosensing element is bonded to an electronics layer, and a junction within the monocrystalline photosensing element includes (in amended claim 1) one of a p-type and an n-type material having a first side adjacent said vertical interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

More specifically, claim 5 is believed allowable at least since it depends from what is believed to be an allowable claim, and for the reasons stated above.

Accordingly, it is believed that the rejection of claim 5 under 35 U.S.C. 103 has been overcome by the amendment and remarks.

REJECTION OF CLAIM 6 UNDER 35 U.S.C. §103

Claim 6 has been rejected under 35 U.S.C. 103 as being unpatentable over Yaung et al. in view of Pan.

The cited Pan reference shows a CMOS image sensor including a via 71 connecting to the gate 32 through polysilicon layer 51, amorphous silicon layer 52, and oxide layer 42. There seems to be issues with the operability as described. Pan implants N-type dopants into polysilicon layer 52 and then P-type dopants "just" near the surface of layer 52 (note the p-n junction is horizontal). Pan then fills the via 71 with metal, which would short-out the p-n junction. If Pan meant to describe a dielectric around via 71, then there would be no movement of electrons from layer 52 to the metal in the via as in the present invention.

Regardless, the present invention differs from the Pan reference in that the p-n junctions are vertical, not horizontal, and the optical sensor is not "blocked" (reduced in area) by the contacts to the p-n junction. Another fundamental difference is in the coupling between the interconnect via and the design/geometry of the photocarrier collection pn junction. In Pan's design, the geometry of the pn junction follows that of the p-implant and contact (anode of photodiode) on the top surface and the via/metal plug forms the photodiode (PD) cathode contact. Since the pn junction shallow (~1000's A) and extends several microns laterally, the photogenerated carriers are collected and separated (i.e. the photodetection process) in primarily a vertical direction. In the present invention, the electrodes are reversed with the interconnect via forming the anode instead of the cathode. The collecting pn junction now follows the contour of the via and it must surround and encompass the entire via (otherwise it would result in shorting of junction). The junction geometry is then a vertially oriented cylinder such that the carrier collection is predominantly in a lateral (radial) direction.

It would not be obvious to one skilled in the art with knowledge of Yeung (a n-p junction formed on the same level as the transistors and the like) and Pan (a shorted via or an insulated via, with a vertical p-n junction) to construct the device of the present invention where a monocrystalline photosensing element is monolithically integrated via a bonding technology to an electronics layer, and a junction within the monocrystalline photosensing element includes (in amended claim 1) one of a p-type and an n-type material having a first side adjacent said vertical interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

More specifically, claim 6 is believed allowable at least since it depends from what is believed to be an allowable claim, and for the reasons stated above

Accordingly, it is believed that the rejection of claim 6 under 35 U.S.C. 103 has been overcome by the amendment and remarks.

REJECTION OF CLAIMS 7-13 AND 15-17 UNDER 35 U.S.C. §103

Claims 7-13 and 15-17 have been rejected under 35 U.S.C. 103 as being unpatentable over Yaung et al. in view of Rhodes.

The Rhodes reference shows a CMOS imager for selectively providing a silicide coating over the transistor gates to improve the speed of the gates. The contact hole 382 merely provides contact from the top of the device to a point below and is surrounded by insulating layer 370. This prevents any lateral movement of carriers as provided by the present invention.

It would not be obvious to one skilled in the art with knowledge of Yeung (a n-p junction formed on the same level as the transistors and the like) and Rhodes (an insulated via) to construct the device of the present invention where a monocrystalline photosensing element

is bonded to an electronics layer, and a junction within the monocrystalline photosensing element includes (in amended claim 1) one of a p-type and an n-type material having a first side adjacent said vertical interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

More specifically, Claim 7 as amended comprises a monocrystalline photosensing element that is bonded to the electronics layer. Furthermore, the junction within the monocrystalline photosensing element now includes (in amended claim 7) one of a p-type and an n-type material having a first side adjacent said vertical interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

Claims 8-13 and 15-17 are believed to be allowable at least for the reason they depend from what is believed to be an allowable claim.

Accordingly, it is believed that the rejection of claims 7-13 and 15-17 under 35 U.S.C. 103 has been overcome by the amendment and remarks.

REJECTION OF CLAIM 14 UNDER 35 U.S.C. §103

Claim 14 has been rejected under 35 U.S.C. 103 as being unpatentable over Yaung et al. in view of Rhodes, and further in view of Mattison et al.

The Mattison et al. reference shows an image sensor array for capturing a sequence of video frames that does not teach any semiconductor process or structure, but merely discloses block diagrams and flow charts.

While claim 14 does claim the electronics circuitry as being optimized for substantial parallel processing of array-captured images, there is no disclosure in either of Yaung et al. as

discussed above, or Rhodes, to suggest the structure of the present invention, or the advantages gained thereby.

It would not be obvious to one skilled in the art with knowledge of Yeung (a n-p junction formed on the same level as the transistors and the like) and Mattison et al (capturing a sequence of video frames) to construct the device of the present invention where a monocrystalline photosensing element is bonded to an electronics layer, and a junction within the monocrystalline photosensing element includes (in amended claim 1) one of a p-type and an n-type material having a first side adjacent said vertical interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

Accordingly, it is believed that the rejection of claim 14 under 35 U.S.C. 103 has been overcome by the amendment and remarks.

REJECTION OF CLAIMS 18 AND 20 UNDER 35 U.S.C. §103

Claims 18 and 20 have been rejected under 35 U.S.C. 103 as being unpatentable over Yaung et al. in view of Rhodes, and further in view of Hosier et al.

The Hosier et al. reference shows a CMOS image sensor array including a plurality of photodiodes and a spillover protection circuit associated with each photodiode. Claim 18 claims a semiconductor structure and does not address any circuitry arrangements as discussed in Hosier et al. Claim 20 claims various materials for the monocrystalline layers of claim 18 and also does not address any circuitry arrangements as discussed in Hosier et al.

It would not be obvious to one skilled in the art with knowledge of Yeung (a n-p junction formed on the same level as the transistors and the like) and Hosier et al. (an image

sensor array with spillover protections for diodes) to construct the device of the present invention where a monocrystalline photosensing element is bonded to an electronics layer, and a junction within the monocrystalline photosensing element includes (in amended claim 1) one of a p-type and an n-type material having a first side adjacent said vertical interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

More specifically, Claim 18 as amended comprises a monocrystalline photosensing element that is bonded to the electronics layer. Furthermore, the junction within the monocrystalline photosensing element now includes (in amended claim 1) one of a p-type and an n-type material having a first side adjacent said vertical interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

Claim 20 are believed to be allowable at least for the reason is depends from what is believed to be an allowable claim.

Accordingly, it is believed that the rejection of claims 18 and 20 under 35 U.S.C. 103 has been overcome by the amendment and remarks.

REJECTION OF CLAIM 19 UNDER 35 U.S.C. §103

Claim 19 has been rejected under 35 U.S.C. 103 as being unpatentable over Yaung et al. and Rhodes in view of Hosier et al. and further in view of Tian et al.

The Tian et al. reference shows an integrated light sensor with a reflective element under each light-sensing element.

Claim 19 teaches adapting the optically active layers to demonstrate sensitivity to different regions of the electromagnetic spectrum.

It would not be obvious to one skilled in the art with knowledge of Yeung (a n-p junction formed on the same level as the transistors and the like) and Hosier et al. (a light sensor with reflective element) to construct the device of the present invention where a monocrystalline photosensing element is bonded to an electronics layer, and a junction within the monocrystalline photosensing element includes (in amended claim 1) one of a p-type and an n-type material having a first side adjacent said vertical interconnect and the other of the one of a p-type and an n-type material adjacent a second side opposed to said first side and positioned horizontally from said first side.

Accordingly, it is believed that the rejection of claim 19 under 35 U.S.C. 103 has been overcome by the amendment and remarks.

CONCLUSION

The remaining cited references have been reviewed and are not believed to affect the patentability of the claims as amended.

No amendment made herein was related to the statutory requirements of patentability unless expressly stated; and no amendment made herein was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

In view of Applicant's amendments and remarks, it is respectfully submitted that Examiner's rejections have been overcome. Accordingly, Applicants respectfully submit that the application, as amended, is now in condition for allowance, and such allowance is therefore

earnestly requested. Should the Examiner have any questions or wish to further discuss this application, Applicants request that the Examiner contact the Applicants attorneys at 480-385-5060.

If for some reason Applicants have not requested a sufficient extension and/or have not paid a sufficient fee for this response and/or for the extension necessary to prevent abandonment on this application, please consider this as a request for an extension for the required time period and/or authorization to charge Deposit Account No. 502,091 for any fee which may be due.

Respectfully submitted,

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